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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/769,721	01/25/2001	Kurt E. Spears	10002651-1	5042

7590 04/23/2007  
HEWLETT-PACKARD COMPANY  
Intellectual Property Administration  
P.O. Box 272400  
Fort Collins, CO 80527-2400

EXAMINER
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AGGARWAL, YOGESH K

ART UNIT	PAPER NUMBER
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2622

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	04/23/2007	PAPER

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**BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES**

**MAILED**

**APR 23 2007**

**Technology Center 2600**

Application Number: 09/769,721  
Filing Date: January 25, 2001  
Appellant(s): SPEARS ET AL.

Augustus W. Winfield  
Reg. No. 34,046  
For Appellant

**EXAMINER'S ANSWER**

This is in response to the appeal brief filed 01/22/2007 appealing from the Office action mailed 09/20/2006.

**(1) Real Party in Interest**

A statement identifying by name the real party in interest is contained in the brief.

**(2) Related Appeals and Interferences**

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

**(3) Status of Claims**

The statement of the status of claims contained in the brief is substantially incorrect. A correct statement of the status of the claim is as follows:

Claims 1 and 4-6 now stand finally rejected as set forth in the final office action dated 09/20/2006, and are the subject of this appeal. The arguments concerning claim 9 were persuasive. Therefore, claim 9 has been allowed.

**(4) Status of Amendments After Final**

No amendment after final has been filed.

**(5) Summary of Claimed Subject Matter**

The summary of claimed subject matter contained in the brief is correct.

**(6) Grounds of Rejection to be Reviewed on Appeal**

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows: claim 9 is allowed.

**(7) Claims Appendix**

The copy of the appealed claims contained in the Appendix to the brief is correct.

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**(8) Evidence Relied Upon**

6,441,851	Yonemoto	08-2002
5,345,319	Yu	09-1994
6,459,077	Hynecek	10-2002

**(9) Grounds of Rejection**

The following ground(s) of rejection are applicable to the appealed claims:

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Yonemoto (US Patent # 6,441,851).

[Claim 1]

A method of scanning comprising exposing an array of photosensors to light, a first time (e.g. long exposure time from t1 to t4 in figure 2)

activating a particular section of a charge transfer gate, where the charge transfer gate has a plurality of sections, each section individually controllable, and fewer than all the sections are activated (e.g. figure 2 shows that during long exposure time, gates V2a and V2b is activated at times t1 and t4 respectively out of the gates V1, V2a, V3 and V2b wherein each section is shown to be individually controllable);

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transferring charges, transferring charges from a contiguous block of the photosensors through the particular section of the charge transfer gate, to a charge shift register (e.g. charges corresponding to photosensors 1 and 2 are transferred to charge shift register during long exposure time at t2 and t4) ,

exposing, the array of photosensors, to light, a second time (e.g. short exposure time from t5 to t8 in figure 2)

transferring charges, from the contiguous block of photosensors through the particular section of the charge transfer gate, to the charge shift register, so that the charges from the contiguous block of photosensors, from more than one exposure, are interleaved in the charge shift register (e.g. charges corresponding to same block of photosensors 11 and 12 are transferred through the same charge transfer gate to the charge shift register and interleaved with the charges from the long exposure time).

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 5 is rejected under 35 U.S.C. 102(b) as being anticipated by Yu (US Patent # 5,345,319).

[Claim 5]

Yu teaches a method of scanning comprising exposing, first (figure 2, blue 5) and second arrays (figure 2, red 3) of photosensors to light, transferring charges, from a first contiguous block of

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photosensors (the blue color array comprises a contiguous first block of photosensors) in the first array of photosensors (figure 2, blue 5), to a charge shift register (figure 2, element 1), wherein the block comprises less than all the photosensors (blue color pixels comprise less than the total number of all the photosensors RGB), and only charges from the first block are transferred; transferring charges from a second contiguous block of photosensors (the red color array comprises a contiguous second block of photosensors) in the second array of photosensors (figure 2, red 3), to the charge shift register (figure 2, element 1, it is noted that the charges are transferred to the same charge shift register as the first block), where only the charges from the second block are transferred, so that charges from contiguous block from more than one array of photosensors are simultaneously interleaved onto the charge shift register (col. 3 line 64- col. 4 line charges from the first block of photosensors comprised of blue color pixels in a first array of photosensors 5 transfer charges to the charge shift registers 1 and the block of red pixels 3 simultaneously comprise less than all the photosensors RGB and these charges are interleaved in the SHIFT register 1. Yu discloses that the signal charges generated in PD arrays 30 and 50 are integrated for a predetermined time period and then shifted to the HCCD analog shift register 10 which would be obvious to one skilled in the art that they are being simultaneously to the charge shift register).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yonemoto (US Patent # 6,441,851) as applied to claim 1 above and in further view of Hynecek (US Patent # 6,459,077).

[Claim 4]

Yonemoto teaches the limitations of claim 1 but fails to teach “.... shifting charges, within the charge shift register, at a lower than normal shift rate”. However Hynecek teaches that these limitations are well known and used in the art (col. 3 lines 35-43). Therefore taking the combined teachings of Yonemoto and Hynecek it would have been obvious to one skilled in the art at the time of the invention to have been motivated to shift charges at a lower than normal shift rate. The benefit of doing so would be to improve the bucket brigade charge transfer efficiency to be similar to that expected of typical CCD devices as taught in Hynecek (col. 3 lines 35-37).

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (US Patent # 5,345,319) as applied to claim 5 above and in further view of Hynecek (US Patent # 6,459,077).

[Claim 6]

Yu teach the limitations of claim 5 but fails to teach “.... shifting charges, within the charge shift register, at a lower than normal shift rate”. However Hynecek teaches that these limitations are well known and used in the art (col. 3 lines 35-43). Therefore taking the combined teachings of Yu and Hynecek it would have been obvious to one skilled in the art at the time of the invention to have been motivated to shift charges at a lower than normal shift rate. The benefit of doing so would be to improve the bucket brigade charge transfer efficiency to be similar to that expected of typical CCD devices as taught in Hynecek (col. 3 lines 35-37).

*Allowable Subject Matter*

8. Claim 9 is allowed.

**(10) Response to Argument**

9. Appellant argues regarding claim 1 that transferring charges, from a contiguous block of the photosensors, through the particular section of the charge transfer gate, to a charge shift register. Yonemoto clearly teaches that charge 1 accumulated at sensor 1 at time t2 is being transferred to a charge shift register (vertical CCD 2) through activation of gate V2a (col. 3 line 55-col. 4 line 4, figures 2 and 3). Then at time t4, the charge 2 is transferred to a charge shift register (vertical CCD 2) through activation of gate V2b (col. 4 lines 5-12, figures 2 and 3).

Therefore, in essence, charges 1 and 2 (a contiguous block of photosensors) are being transferred at times t2 and t4 by activating charge transfer gates V2a and V2b (a particular section of the charge transfer gate) through the charge transfer gates V2a and V2b ( the particular section of the charge transfer gate) to a charge shift register.

Thus the claim limitation “activating a particular section of a charge transfer gate, where the charge transfer gate has a plurality of sections, ..... transferring charges, transferring charges from a contiguous block of the photosensors through the particular section of the charge transfer gate, to a charge shift register” is clearly being taught by Yonemoto.

The appellant further argues that the charges 1 and 2 are transferred at two different times through two different sections. The Examiner respectfully disagrees. The claim never recites that the charges have to be transferred at the same time or are being simultaneously transferred. Therefore, the charges 1 and 2 being transferred at times t2 and t4 accumulated over a long period of time meets the claim limitations.



Appellant's arguments regarding charges being transferred through two different sections of the charge transfer gates V2a and V2b, the Examiner reads V2a and V2b as a particular section of a charge transfer gate. The claim in no way limits a particular charge transfer section to have only one charge transfer gate. The term "a particular section of the charge transfer gate" does not imply to one skilled in the art to have only have only one charge transfer gate. It is broad enough to interpret V2a and V2b as a particular section of a charge transfer gate.

Therefore, in response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., charges have to be transferred at the same time or are being simultaneously transferred through only one charge transfer gate) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

10. Appellant argues with regards to claim 5 that Yu does not teach interleaving charges from contiguous blocks from more than one array of photosensors on one charge shift register. Yu teaches charges from contiguous blocks from more than one array of photosensors (figure 2, blue 5 and red 3) being interleaved into one charge shift register (Horizontal CCD 1):

Appellants main argument is that HCCD 1 is a pair of different charge registers, namely upper and lower shift registers and not one shift register. The Examiner reads HCCD 1 as one charge transfer register having upper and lower pair of charge shift registers. Nothing in the claim limits a charge shift register to have only one shift register. One skilled in the art would not interpret the claim term "a charge shift register" to have only one charge shift register i.e. it is broad enough to read HCCD 1 as a charge transfer gate.

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Therefore, in response to appellant's argument that the references fail to show certain features of appellant's invention, it is noted that the features upon which appellant relies (i.e., a charge shift register to have only one shift register) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

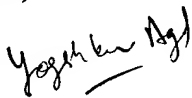
**(11) Related Proceeding(s) Appendix**

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Yogesh K. Aggarwal



Examiner

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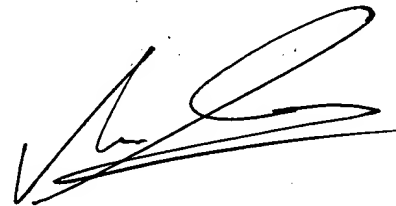
YKA

April 12, 2007

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